Abstract—In this paper we use the load current of the CPU as decision of the working state of the PC is either a heavy load or a light load. Based on the voltage specification of each device on the PC motherboard, we use the current control for dynamic voltage scaling (IREF-DVS) regulator to provide different voltages for each device. When the PC has a light load we can decrease the operating voltage of each device to the minimum voltage, and with a heavy load this design can increase it to the maximum voltage to improve the performance.

I. INTRODUCTION

There are a lot of devices on the PC motherboard, and they all need power to work properly. The CPU is the most power-hungry component. With an Intel 17-870 CPU the maximum current of the core voltage is 110A, and the maximum power consumption is 95W. So there are many studies currently being made to find a way reduce the PC power consumption. These studies focus on reducing the core voltage to reduce power consumption of the CPU.

In the ACPI specifications the CPU power-saving technology is called C-State [1]. The C-State is defined as the S0 state, the CPU idle state, and thus it is defined as one of the PC working states. Table I shows all definitions of the C-State. When the CPU enters into the C-State, the C1-State and the C3-State both stop the internal CPU clock. The difference is that the CPU can also control the internal cache memory in the C1-State but not in the C3-State because the internal PLL circuits and the cache memory are all shut down in the C3-State. When these units are stopped, it means that the CPU is in the sleep mode. But merely only cutting off the internal clock signals is not enough to further reduce CPU power consumption. Therefore the next step is to reduce the processor voltage. We know that power consumption is proportional to voltage. If we can reduce the CPU operating voltage, this will reduce the CPU power consumption. The C6-State is a deep sleep mode which reduces the CPU operating voltage for lower power consumption.

When the CPU goes into the C6-State, this state allows the reduction of power consumption by reducing the CPU core voltage, even to as low as 0V. At this time, the CPU is in a complete sleep state because the CPU has a special internal static memory cell. The CPU writes all information into the static memory cell when it exits from the C6-State, thus ensuring that the previous work is not lost.


different CPU C-States:

\[
P_{C_0} > P_{C_1} > P_{C_3} > P_{C_6} \tag{1}
\]

Below is the comparison of the resumption time from each C-State to the C0-State:

\[
T_{C_6 \rightarrow C_0} > T_{C_3 \rightarrow C_0} > T_{C_1 \rightarrow C_0} \tag{2}
\]

Fig. 1 is the transition of the CPU C-States. The CPU can go into any C-State for the best performance and power saving. The C6-State can only adjust the core voltage of the CPU but not the operating voltage of the other devices in the PC system.

Dynamic Voltage and Frequency Scaling (DVFS) are currently most commonly used to enhance the CPU performance, and the power saving technologies C-State and Intel Turbo Boost [2] both use DVFS. DVFS dynamically adjusts both the CPU clock frequency and the operating voltage. The frequency and voltage can be adjusted upward to enhance performance and adjusted downward to save power. The Turbo Boost function adjusts the voltage upward with the CPU frequency to improve performance. The C-State reduces the CPU operating frequency and voltage to reduce power. There are many technologies related to Dynamic Voltage Scaling (DVS), such as Process-Driven DVS [3], Application-Driven DVS [4], Temperature-Aware DVS [5][6] and Energy-Aware DVS [7]. These methods determine the voltage operating point, which usually depends on the CPU operating frequency or the operating temperature.
Battery-Aware DVS [8][9] is used in portable products for longer use.

Every PC motherboard device needs a power supply to provide power to work correctly, and each device has its own specifications for voltage. For example, the standard DDRIII-VDD voltage is 1.5V, but there is an acceptable voltage margin. In the DDRIII specifications the operational voltage range of DDRIII-VDD is defined at 1.425V - 1.575V. In other words, DDRIII devices can work well as long as the voltage source is maintained at 1.425V or above. Before designing the voltage regulation system we must first understand each voltage range of the device to make sure it can work well.

Table II is the power deliver list of the motherboard [10]. It defines the working current and operating voltage range of all on-board devices. If the motherboard can lower the voltage in a high-consumption device, it saves more power.

Equation (3) is a known formula for power consumption. Power consumption is proportional to voltage and operating current. Assuming the current is a constant, decreasing the voltage is the easiest method for power saving.

\[ P = I \times V \]  

In PC motherboard design specifications the operating voltage of all devices has a design margin. We can adjust the voltage down to the minimum of the margin to save power, and the operating voltage lets the PC work even in the worst possible scenario. For example, the standard working voltage of CPU-VTT is 1.1V, assuming the operating current is 30A. If the PC motherboard lowers the voltage to 1.045V, it saves power as below.

\[ P_{\text{SAVE}} = P_{\text{V\_type}} - P_{\text{V\_min}} \]  
\[ P_{\text{SAVE}} = P_{1.1V} - P_{1.045} \]  
\[ P = [1.1V \times 30A] - [1.045V \times 30A] = 1.65W \]

If \( P_{\text{SAVE}} \) is used in portable products, a device saving 1.65W means that its use can be extended by up to 5% with the same battery capacity.

As a PC is usually seldom under heavy loading operating conditions, even the operating time of light loading will be much larger than the operating time of heavy loading. In [11][12] it is pointed out that both workload and load current have a very strong correlation.

When the PC runs high-performance requirement software, for example, a 3D game, the CPU has to carry out a high speed floating operation which requires a relatively large source current. When the PC is running under low performance conditions, for example, MSN or idling, the CPU is in the idle state. The current requirement of the CPU is now relatively low, and we can therefore use the Accurate Current Monitor (IMON) function of the DC-DC buck converter [13]. It is easy to get the CPU operating current and then estimate the current system running state. IMON is an analog signal proportional to the load current of the CPU \( V_{\text{CORE}} \); it is a voltage output representation (\( V_{\text{IMON}} \)). When the load current of the \( V_{\text{CORE}} \) changes, then the \( V_{\text{IMON}} \) changes. The \( V_{\text{IMON}} \) is relatively lower when the load current of the \( V_{\text{CORE}} \) decreases relatively higher when the load current of \( V_{\text{CORE}} \) increases. The \( V_{\text{IMON}} \) change curve is close to linear; it shows a voltage between 0V-1.V. Fig. 2 shows that load current and \( V_{\text{IMON}} \) both are proportional to changes in real-time and are synchronized.
The devices on the PC motherboard mostly use a DC-DC buck converter to provide a voltage source. The DC-DC buck converter output voltage value (V_{OUT}) is determined by the feedback voltage (V_{FB}). Fig. 3 shows how the DC-DC buck converter adjusts the output voltage. Assuming that the required device operating voltage is 1.2V, we should make sure that the V_{OUT} is fixed at 1.2V. There is an internal reference voltage (V_{REF}) in the controller of the DC-DC buck converter which is a fixed voltage of 0.8V. We match the V_{OUT} by \( \frac{R_2}{(R_1 + R_2)} \) and get the V_{FB} = 0.8V. If we want to change the V_{OUT}, we just change the V_{FB}.

We propose a new method to reduce the system level power consumption of a PC by which we lower the operating voltage of devices. We can easily obtain the necessary CPU load current by V_{IMON} and then ascertain the CPU working state. For all devices we can increase the operating voltage if the CPU works in high-performance status, thus making the PC system more stable, and we can decrease it if the PC works in a low-performance status, thus reducing the PC system power consumption.

We have designed a circuit that dynamically changes the input reference voltage V_{FB} according to the V_{IMON}. This circuit easily changes the DC-DC Buck Converter output voltage V_{OUT}. Based on the voltage characteristics of the different devices the control circuit makes adjustments, because their voltage operation ranges are not identical. Fig. 4 is the circuit of the IREF-DVS Regulator circuit. There is an IREF-Generator in the IREF-DVS, so we can sink or source the I_{REF} current in the V_{FB} pin to change the V_{OUT}. If we want the V_{OUT} to be higher, we let the IREF-Generator sinks the I_{REF} in the V_{FB} pin. The V_{FB} then decreases with the I_{REF} current, and the V_{OUT} increases. If we need a lower V_{OUT}, we let the IREF-Generator source the I_{REF} in the V_{FB} pin. The V_{FB} then increases with the I_{REF} current, and the V_{OUT} decreases.

**II. DESIGN OF THE IREF-DVS REGULATOR**

Fig. 5 shows the schematics of the IREF-Generator. There is a group of 8-bit target-voltage setting inputs, a decoder and a set of internal current generators. We set the V_{OUT} through the 8-bit input value. The 8-bit V_{OUT} is decoded by the decoder. The V_{OUT} is converted to I_{REF} into a current generator. The current generator is an adjustable current sink/source which can adjust the I_{REF} current upward or downward. Through the SMBus of the motherboard we control the IREF-Generator. We depend on the V_{IMON}, set 3 trigger-points and 4 steps of the V_{OUT}, and let the V_{OUT} change in steps.

Fig. 6 is the flow chart of the IREF-DVS. We use the SMBus interface of the PC motherboard to control the IREF-DVS. With the SMBus it is easy to control both the size and the direction of the I_{REF}. When we need to decrease the output voltage, the motherboard BIOS reads the trigger-points of the V_{IMON} and the voltage step values through the SMBus. Nest the decoder of the IREF-Generator turns on the top of the current source array. Its source current increases the V_{FB}, and the V_{OUT} decreases. To increase the output voltage, the motherboard BIOS reads both the trigger-points of the V_{IMON} and the voltage step values through the SMBus. Next the decoder of the IREF-Generator turns on the bottom of the current sink array. The IREF-Generator sinks the current to decrease the V_{FB}, and the V_{OUT} increases. In addition, when the V_{IMON} changes up and down in real-time, according to its three trigger-points, the V_{OUT} changes synchronously.
Fig. 7 shows the relationship between $V_{\text{IMON}}$ and $V_{\text{OUT}}$ after using the IREF-DVS. When the PC runs a program, the CPU load current increases and changes dynamically, and the voltage of the $V_{\text{IMON}}$ also increases and changes with the CPU load current. When the IREF-DVS senses that the $V_{\text{IMON}}$ should change upwards, it means that as the PC is currently running on a high-performance program, a higher operating voltage is needed to improve the working performance. Therefore the sinking of the current in the VFB by the IREF-DVS causes the $V_{\text{OUT}}$ to increase. When the program is finished, the CPU operating current drops, the $V_{\text{IMON}}$ also decreases, and when the IREF-DVS senses that the $V_{\text{IMON}}$ should change downward, it means that the PC currently does not require an operating voltage for a high-performance program. Therefore the sourcing of the current in the VFB by the IREF-DVS causes the $V_{\text{OUT}}$ to decrease, thus saving power.

### III. EXPERIMENTATIONS

In this experiment we have used two independent groups of IREF-DVS Regulators and have selected two different operating voltages of the Devices on a PC motherboard {CPU-VTT, DDRIII-VDD}. Now we can verify the power saving improvements in this test PC.

Table III: Relationship between CPU Loading and $V_{\text{IMON}}$

<table>
<thead>
<tr>
<th>Test Condition</th>
<th>$V_{\text{IMON}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Win XP only (CPU Loading 2%)</td>
<td>59.9mV</td>
</tr>
<tr>
<td>CPU Loading 25%</td>
<td>509mV</td>
</tr>
<tr>
<td>CPU Loading 50%</td>
<td>710mV</td>
</tr>
<tr>
<td>CPU Loading 75%</td>
<td>910mV</td>
</tr>
<tr>
<td>CPU Loading 100%</td>
<td>1.05V</td>
</tr>
</tbody>
</table>

Fig. 8 is the block diagram of our test PC motherboard and the two devices with independent IREF-DVS regulators. We use Windows XP with Prime95 to find the relationship between CPU loading and $V_{\text{IMON}}$. The five test conditions of the CPU loading are 2% (Windows XP only), 25%, 50%, 75%, and 100%.
75%, 100%. Before using the IREF-DVS regulators we have measured the $V_{\text{IMON}}$ and the operational currents of the devices under the five test conditions. As shown in Table III, when the CPU loading changes from 2% to 25%, the $V_{\text{IMON}}$ shows a great change. The proposed design can save on the power consumption of CPU-VTT and DDRIII-VDD with IREF-DVS regulators when the CPU loading is less than 75%.

We have first measured the relationship between the $V_{\text{IMON}}$ and the operating voltages of the two devices. In Fig. 9, we observe the operational voltage without IREF-DVS regulators, where the two voltages are maintained at the original level \{CPU-VTT, DDRIII-VDD\} = \{1.1V, 1.5V\}, not changing with the $V_{\text{IMON}}$. When using the IREF-DVS regulators, the two operational voltages change with the $V_{\text{IMON}}$, in real-time, as shown in Fig. 10. Table IV shows the settings of the three $V_{\text{IMON}}$ trigger-points \{244mV, 488mV, 976mV\} and the four-step supply voltages of the two devices on our test motherboard.

### IV. TEST RESULT

Normally, when a PC is operating the CPU loading always changes with the program action. To understand the performance and the power consumption with IREF-DVS regulators we have measured the total power consumption on a test PC under the four conditions below.

1. Idle in Win XP (Not running any program)
2. Play DVD (Windows Media Player)
3. 3DMark06
4. Restaurant City @ Facebook

We have measured the power consumption on a 12V power rail which is the input power for the CPU and the DDR. Fig. 11 is the comparison of the average power consumption of devices without IREF-DVS regulators and with IREF-DVS regulators under the four test conditions. Fig. 11 shows how the IREF-DVS regulators improve the power consumption under all conditions.

![Fig. 11. Comparison of average power consumption with and without IREF-DVS regulator.](image)

<table>
<thead>
<tr>
<th>$V_{\text{IMON}}$</th>
<th>CPU-VTT Voltage</th>
<th>DDRIII-VDD Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 - 244mV</td>
<td>1.045V</td>
<td>1.425V</td>
</tr>
<tr>
<td>244 - 488mV</td>
<td>1.065V</td>
<td>1.450V</td>
</tr>
<tr>
<td>488 - 976mV</td>
<td>1.080V</td>
<td>1.475V</td>
</tr>
<tr>
<td>976 - 1100mV</td>
<td>1.100V</td>
<td>1.500V</td>
</tr>
</tbody>
</table>

Fig. 12 is the performance score of 3Dmark06. We observe that the performance score is not markedly different between devices that here and do not have IREF-DVS regulators.

![Fig. 12. Performance score of 3Dmark06.](image)
V. CONCLUSION

In our design the working current of the actual monitoring CPU changes the device voltage. The device voltage changes in real-time and according to the real CPU working state. Power saving is at the system level. Through the SMBus control the proposed design sets the voltage steps and trigger-points. When the operating voltage in the device follows the specifications, it sets a dynamically change the voltage to the most power-saving mode. The test results show that through the IREF-DVS regulator this design reduce power consumption by more than 2W, an improvement of about 5%. In the future we will try to change the device voltage to less than operating voltage specifications to achieve even greater power saving.

REFERENCES


