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Using a Hybrid LDO Regulator and a Switching Regulator Circuit to Reduce the Power Consumption in the Light Load Operation of a Server Motherboard

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***Abstract*—In this paper we propose a hybrid LDO regulator and switching regulator circuit design that uses an LDO regulator instead of a switching regulator to operate in light load. By means of this method our design reduces the power consumption of a switching regulator in light load at the input terminal, and then reduces the power consumption of the server motherboard during the operation. This design includes a microcontroller Unit (MCU) which is able to initialize, detect, judge and control both regulator operations. In addition, the MCU controls both the LDO regulator and the switching regulator in order to transition between light load and heavy load.**

I. INTRODUCTION

At present the power saving technology called Intelligent Power Technology Node Manager is mostly used in the server motherboard [1]. This technology, which uses integrated power gates, reduces individual idling cores to near zero power. These power gates can be controlled either manually or through automated settings that adjust the Central Processing Unit (CPU) and the Registered Dual In-line Memory Module (RDIMM) to the lowest available power state to meet workload requirements without impacting performance. This technology is helpful to reduce operating power consumption and can be of help to meet power saving goals. Besides, another method uses the multi-phase Pulse Width Modulation (PWM) voltage regulator of dynamic power management for the CPU core voltage. This regulator, which is able to sense the CPU workload and current consumption, automatically adjusts the CPU core voltage and operating frequency to meet the motherboard power saving goals [2] [3]. Both methods, which are useful power saving methods, are used in conjunction with CPUs and RDIMMs. But on the server motherboard there are other controllers that need power sources from an LDO regulator or a switching regulator and these controllers will initiate power consumption when needed by these regulators. According to the previous design, an LDO regulator has the advantages of linear adjustment, low ripple, low noise, low quiescent current and fast transient response [4][5], but it has poor power conversion efficiency. As the excess energy is converted into heat and cannot provide a greater current output, the LDO regulators are used mostly to meet the small current requirements of controllers. Although the switching regulator shortcomings are a large output ripple, electromagnetic interference (EMI) and slow transient response problems, but its advantages are larger current output capability and higher conversion efficiency which used in heavy load operation. When the switching regulator is in light load operation, due to gate drive loss with switching loss the result is a switching regulator with lower efficiency [6][7]. In keeping with both an LDO regulator and a switching regulator with different characteristics, we redesign the regulator output terminals that are dependent on different load conditions and the power consumption of the input terminal impact. Our experiment results show that when the output terminal load is less than 0.18A, the input terminal current consumption of the LDO regulator is better than that of a switching regulator. On the other hand, when the output terminal load is more than 0.18A, the switching regulator input terminal current consumption as the load increases will obviously be less than the LDO regulator. Because of this result, in this paper we propose a hybrid LDO regulator and a switching regulator circuit designed to supply the power source of the server motherboard. When the current load is less than 0.18A, the power source is supplied from the LDO regulator; when the current load is more than 0.18A, this design will switch to the power source supplied from the switching regulator. This design achieves the purpose of improving the efficiency of the power consumption on the server motherboard.

The organization of this paper is as follows. In Section II, we analyze both the LDO regulator and the switching regulator. In Section III, we present the design of the circuits and measurement. In Section IV, we draw the conclusions.

II. AN ANALYSIS OF BOTH THE LDO REGULATOR AND THE SWITCHING REGULATOR

The power management interface of the server motherboard is based on the ACPI (Advanced Configuration and Power Interface) specification definitions that can be divided into five states S0 (system normal working state)/S1 (low wake latency sleeping state)/S3 (suspend to RAM state)/S4 (suspend to disk state)/S5 (soft off state) [8]. The server belongs to an uninterrupted terminal service system, so the most common operation is in the S0 state. Some studies explore the use of a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) to cut off standby power in the S3/S4 state in order to reduce power consumption [9]. This

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approach, which is an effective way to reduce system power consumption, has only a limited effect on the server system as server systems rarely operate in the S3/S4 state. Therefore this paper explores the regulators of the server motherboard. Many research papers have been written on the improvement of the regulators transient response time, efficiency, output ripple or EMI reduction [10-12]. This design uses either an LDO regulator or a switching regulator at the input terminal (+3.3V) current consumption. In Fig. 1, which shows a typical LDO regulator and a group of switching regulator circuits, we connect current meters in series between the input terminal and the MOSFET of the regulators. The output terminal (+1.8V) is connected to the Direct Current (DC) loader with the loading settings from 0A to 1A, through the output terminal load in order to judge and switch the input terminal power sources of both regulators.

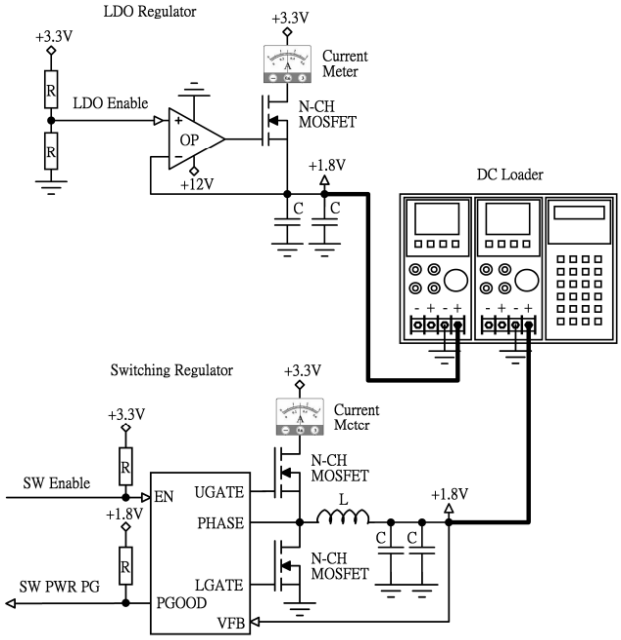

Fig. 1. A typical LDO regulator and a switching regulator circuits

Fig. 2 shows an LDO regulator and a switching regulator in the output terminal DC loader current set from 0A to 1A with the input terminal current consumption analysis curve. In these curves of the input terminal current consumption, the black line represents the current consumption of an LDO regulator and the blue line represents the current consumption of a switching regulator. The curves show the difference of the input terminal current consumption.

As in Table I, we sort out the input terminal current consumption of an LDO regulator which is less than that of a switching regulator. When the output terminal load is 0A, the LDO regulator input terminal current consumption is 0A and the switching regulator has consumed 0.079A. When the output terminal load is set to 0.1A, 0.15A, 0.16A, 0.17A and 0.18A, the input terminal current consumption of the LDO regulator is less than the switching regulator by about 0.037A, 0.014A, 0.01A, 0.006A and 0.001A. The analysis results prove that when the output terminal is in the light load condition, the input terminal current consumption of the LDO regulator is less than the switching regulator.

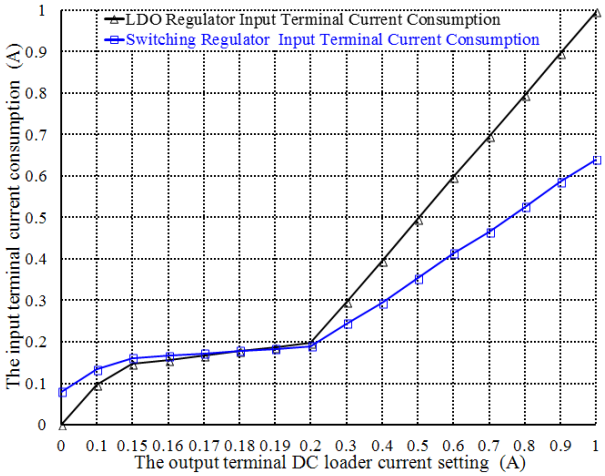

Fig. 2. The current consumption analysis curve of the LDO regulator and the switching regulator in the input terminal

TABLE I
THE INPUT TERMINAL CURRENT CONSUMPTION DIFFERENCE OF THE LDO REGULATOR AND THE SWITCHING REGULATOR

The output terminal (+1.8V) DC loader current setting	LDO regulator input terminal (+3.3V) current consumption	Switching regulator input terminal (+3.3V) current consumption	LDO regulator input terminal current consumption saving
0A	0A	0.079A	0.079A
0.1A	0.096A	0.133A	0.037A
0.15A	0.147A	0.161A	0.014A
0.16A	0.156A	0.166A	0.01A
0.17A	0.166A	0.172A	0.006A
0.18A	0.177A	0.178A	0.001A

III. CIRCUIT DESIGN AND MEASUREMENT

According to the comparison of Section II, this design proposes a hybrid LDO regulator and a switching regulator circuit design that has the following characteristics: when the output terminal is a light load, the input terminal current consumption of the LDO regulator is less than the switching regulator. When the output terminal is a heavy load, the input terminal current consumption of the switching regulator is less than an LDO regulator. This design uses an LDO regulator to replace a switching regulator with a light load to supply a power source to the controllers. When the operation of the controllers is a heavy load, the power source supply from an LDO regulator may change to a switching regulator. This design detects the current consumption of an input terminal and automatically swaps both the LDO regulator and the switching regulator in light load or heavy load operation. By means of this design we can reduce the server motherboard power consumption. Fig. 3 is the block diagram of the circuit design. In addition to the common LDO regulator and the switching regulator, our design also includes a current load detector circuit, an ORING diode [13] and the MCU. The current load detector circuit is used to

detect the input terminal current consumption status of the regulator. When it detects the input terminal current consumption according to this design target, it will trigger a signal to the MCU. The ORING diode will be connected in series between the regulator output terminal and the controller, and can be used to isolate the voltage when both regulators are operating simultaneously. The MCU is used to monitor and control the LDO regulator and the switching regulator by means of automatic swapping.

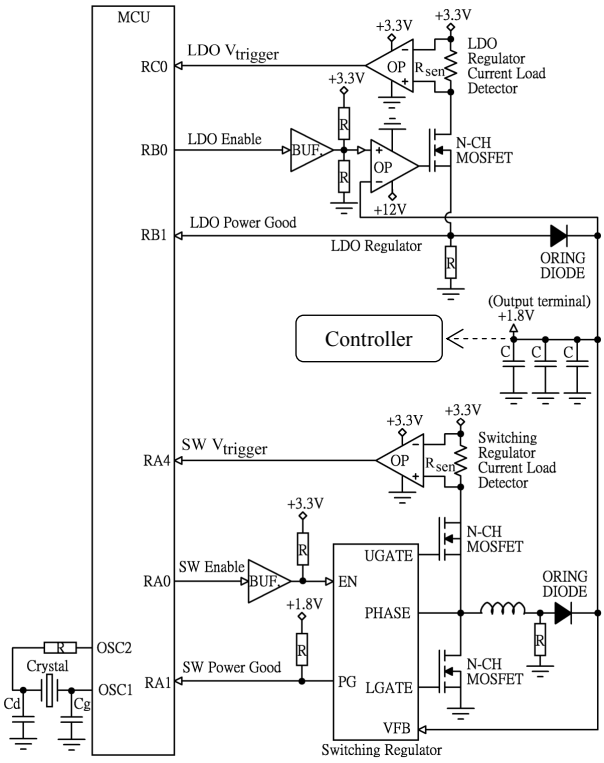

Fig. 3. The block diagram of both the hybrid LDO regulator and the switching regulator circuits

A. *The Current Load Detector Circuit*

The current load detector circuit is shown in Fig. 4. It consists of an operational amplifier (OP amp) and a precision power resistor (R_{sen}). The OP amp is used to determine the voltage difference between V_{source} and V_{drop} in order to decide $V_{trigger}$. In our design, when $V_{drop}=V_{source}$, the output of $V_{trigger}$ is high, when $V_{drop}<V_{source}$, the output of $V_{trigger}$ will transit to low. The precision power resistor is based on the input load current (I_{load}) to generate the voltage consumption (V_{load}). Therefore if the value of the I_{load} becomes large, the value of V_{load} also will become large. Equation (1) shows the load current detector circuit how to decide V_{drop} and determine the input terminal current consumption to achieve the target set by this design.

$$V_{drop}=V_{source}-V_{load}$$
$$=V_{source}-(I_{load}\times R_{sen}) \quad (1)$$

According to Table I, as 0.18A is the cross over point in the input terminal current consumption of both an LDO regulator and a switching regulator, this design set I_{load} in 0.18A as the maximum value. And as the V_{source} and the V_{drop} are more than the 0.2V voltage gap, this difference can make OP amp transitions. Therefore this design sets the value of the V_{load} as 0.2V which decides the value of the R_{sen}. As in Equation (2), the calculation result decides the value of the R_{sen} set to 1.1Ohm. According to equation (1) (2), when I_{load} has achieved 0.18A of this design goal, as the V_{drop} will drop down to 3.102V, then the OP amp $V_{trigger}$ output transit will be low and inform the MCU to begin swapping.

$$R_{sen}=\frac{V_{load}}{I_{load}}$$
$$=\frac{0.2V}{0.18A}=1.1Ohm \quad (2)$$
$$V_{drop}=3.3V-(0.18A\times 1.1Ohm)$$
$$=3.102V \quad (3)$$

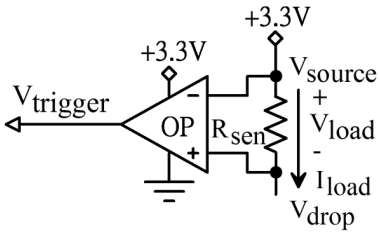

Fig. 4. The current load detector circuit

The current load detector circuit switching waveform measurement is shown in Fig. 5. When the V_{drop} is less than the V_{source} as there is about a 0.2V voltage gap, and as the $V_{trigger}$ transit to low, the results show that this detector circuit meets the design target.

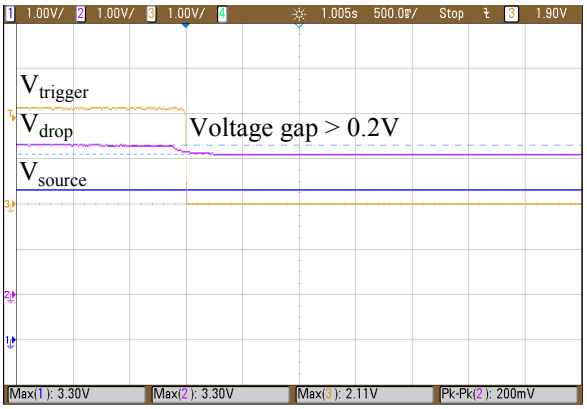

Fig. 5. The current load detector circuit switching waveform

B. *The ORING Diode Circuit*

This design uses both an LDO regulator and a switching regulator. The input terminal power consumption is based on the detection of the light load or heavy load. The current load detector, which detects the load of the controller, decides when to swap the operation of both regulators to supply a power source to the controller. This design connects both regulator output terminals to the same power source of the

controller input terminal. In order to prevent the interaction of both regulator operations, we used one direction turned on as a low forward voltage (VF) by means of a Schottky diode which is in series with the output terminal of the regulator. Both regulators are in parallel output to the power source of the controller input terminal. This kind of application is called the ORING diode, whose circuit is as shown in Fig. 6. The ORING diode is mostly used at the N+1 redundant power supply module, to prevent a different power supply module output current flow from going to another power supply module. The result would be an unstable system operation. If any one power supply module is at fault, another power supply module will be able to continue as a supply power source to system [14] [15]. Due to this design concept of regulators which is similar to the N+1 power supply module, we used an ORING diode for this design.

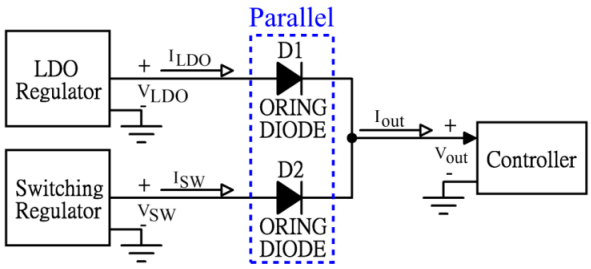

Fig. 6. The ORING diode circuit

Table II shows the operation relationship of both regulators when utilized with an ORING diode as in this design. When only an LDO regulator is enabled, D1 is forward and turned on, and D2 is reversed and cut off. When only a switching regulator is enabled, D2 is forward and turned on, and D1 is reversed and cut off. When the LDO regulator is swapped to the switching regulator, D1 will continue to be turned on until the switching regulator operates normally. After the LDO regulator is disabled, D1 will be reversed and cut off, and D2 will be turned on at the same time. When the switching regulator is swapped to the LDO regulator, D2 will continue to be turned on until the LDO regulator operates normally. After the switching regulator is disabled, the D2 will be reversed and cut off and the D1 will be turned on at the same time. By use the ORING diode isolation we can ensure that both regulators will operate normally in this design and won't affect the operation of the controller.

TABLE II
REGULATORS WITH ORING DIODES OPERATED RELATIONSHIP

Regulators Operation	D1	D2
Only LDO Regulator Enabled	Turned ON	Cut OFF
Only Switching Regulator Enabled	Cut OFF	Turned ON
When LDO Regulator is swapped to Switching Regulator output	Turned On -> Cut OFF	Cut OFF -> Turned ON
When Switching Regulator is swapped to LDO Regulator output	Cut OFF -> Turned ON	Turned On -> Cut OFF

C. *The MCU Control Circuit*

The MCU is the control kernel of this design; it is used both to power on the initial set and to detect the current load detector trigger and the swap function when both regulators are operating. Besides, the MCU internal timer is used to count the trigger signal of the current load detector, which verifies whether this trigger signal meets the setting time of this design. This timer uses an external crystal as the MCU clock reference [16]. This design is as shown in Fig. 3 supplies the power source from the LDO regulator when swapped to the switching regulator as shown in the MCU operation flow chart in Fig. 7. After the power is on, the MCU initially sets the LDO regulator to be enabled (LDO Enable) and the switching regulator to be disabled (SW Disable). The controller, which originally is operating from a light load when subsequently becomes a heavy load, and then is supplied by the LDO regulator to meet this design target. The current load detector of the LDO regulator will, therefore, trigger a low signal (LDO $V_{trigger}$= Low) to the MCU, which the internal timer will begin counting. If the time interval of this low signal is shorter than 1s, the MCU will maintain the operation of the LDO regulator; if the interval is longer than 1s, the MCU will enable the switching regulator (SW Enable). Moreover, the MCU will also detect the power good signal of the switching regulator (SW Power Good). If a low signal is received that means the switching regulator is not operating normally and the MCU will still keep the operation of the LDO regulator. If a high signal is received, which means the switching regulator is operating normally, the MCU will disable the LDO regulator (LDO Disable).

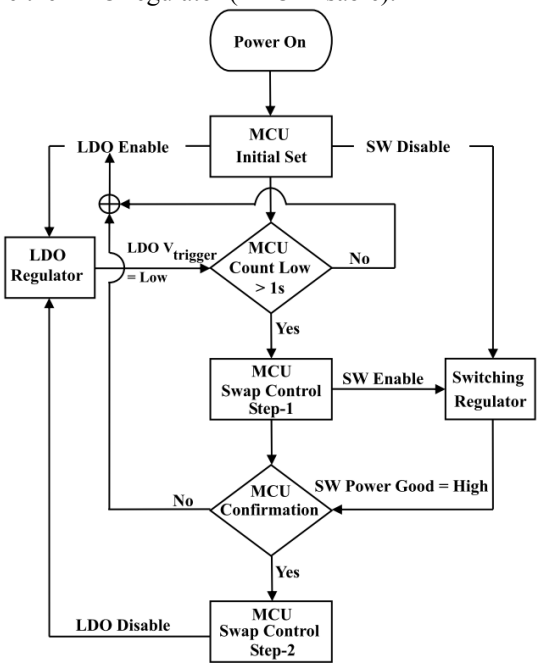

Fig. 7. The MCU control flowchart for power on and the LDO regulator swapped to the switching regulator

Fig. 8 shows the real waveform measurement. After the power is turned on, the MCU initially will set the LDO regulator to be enabled and the switching regulator to be disabled. The controller power source will be supplied from the LDO regulator.

Fig. 9 shows the MCU how to control the LDO regulator swap to the switching regulator real waveform measurement.

The waveform shows when the current load detector of the LDO regulator triggers the low signal longer than 1s to the MCU, the MCU will enable the switching regulator. After receiving a power good signal, the MCU will disable the LDO regulator. Then, the switching regulator will supply a power source to the controller.

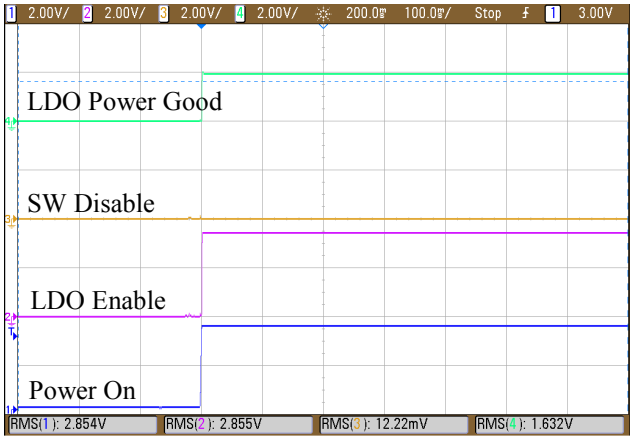

Fig. 8. The MCU initial set waveform after power on

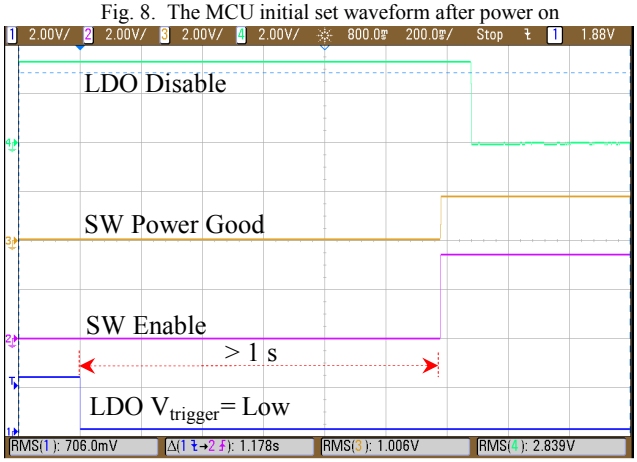

Fig. 9. The MCU controls the LDO regulator swap to the switching regulator waveform

Fig. 10 shows that when the controller operates from the heavy load back to the light load, and the switching regulator input terminal light load meets this design setting, the current load detector of the switching regulator will trigger a high signal (SW V$_{trigger}$= High) to the MCU, which the internal timer will begin counting. If this high signal is shorter than 1s, the MCU will continue the operation of the switching regulator; if the signal is longer than 1s, the MCU will enable the LDO regulator. Moreover the MCU will also detect the power good signal of the LDO regulator (LDO Power Good). If a low signal is received that means the LDO regulator is not operating normally, and the MCU will still maintain the operation of the switching regulator. If a high signal is received that means the LDO regulator is operating normally and the MCU will disable the switching regulator.

Fig. 11 shows how the MCU controls the switching regulator swap back to the LDO regulator real waveform measurement. As shown in the waveform, when the current load detector of the switching regulator triggers a high signal to the MCU which is longer than 1s, the MCU will enable the LDO regulator. After a power good signal is received, the MCU will disable the switching regulator. Then, the LDO regulator will supply a power source to the controller.

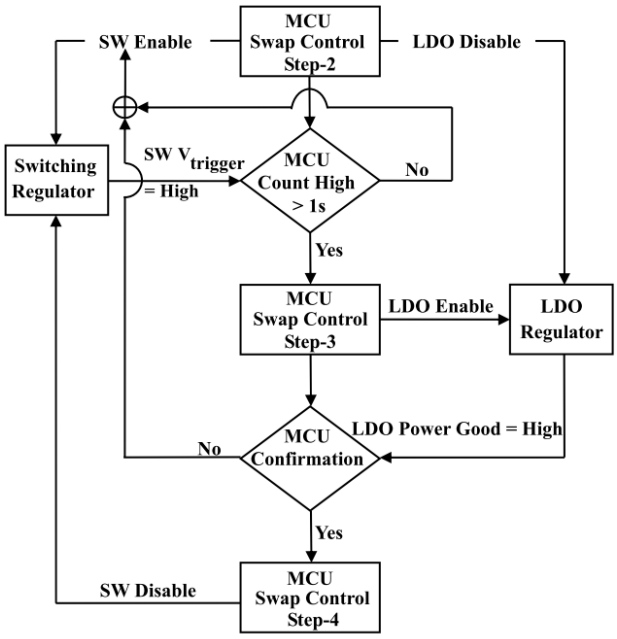

Fig. 10. The MCU control flowchart for the switching regulator as swapped to the LDO regulator

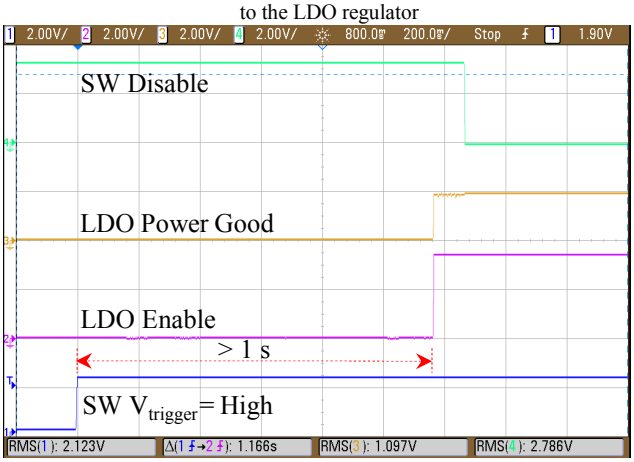

Fig. 11. The MCU controls the switching regulator swap to the LDO regulator waveform

A comparison between the original design and this design at the input terminal current consumption is shown as Table III. This design includes an experiment of the CPU Power Voltage Phase Locked Loop (PVPLL) and the Serial Attached SCSI (SAS) controller power sources at the server motherboard. Their +1.8V power sources are supplied from the switching regulators. We measure the input terminal current consumption in light load. In the original design the CPU PVPLL consumes 0.134A; with the SAS controller it consumes 0.167A, but in our design the CPU PVPLL consumes 0.095A and with the SAS controller it consumes 0.155A. From the experiment results we will note that this

design at the input terminal power consumption is reduced by 0.1683 watt. The percentage of improvement is 16.94% as shown in equation (4) (5). In addition, this design also has other advantages as shown in Table III. This hybrid circuit design which uses the LDO regulator operates in light load to supply the power source. Because the LDO regulator's MOSFET operates in a saturation region rather than as a switch application, the output terminal power source has the advantages of lower output ripple, noise and faster transient response.

$$\begin{aligned}\text{Power Consumption}_{\text{reduce}} &= P_{\text{Original Design}} - P_{\text{Hybrid Design}} \\ &= [3.3\text{V}\times(0.134\text{A}+0.167\text{A})] - [3.3\text{V}\times(0.095\text{A}+0.155\text{A})] \\ &= 0.1683 \text{ watt} \end{aligned} \quad (4)$$

$$\begin{aligned}&\text{Power Consumption Improvement\%} \\ &= \frac{\text{Power Consumption}_{\text{reduce}}}{P_{\text{Original Design}}} \times 100\% \\ &= \frac{0.1683 \text{ watt}}{3.3\text{V}\times(0.134\text{A}+0.167\text{A})} \times 100\% \\ &= 16.94\% \end{aligned} \quad (5)$$

TABLE III
A COMPARISON BETWEEN THE ORIGINAL DESIGN AND THIS DESIGN IN LIGHT LOAD CONDITION

Original design on the server motherboard				
Power Source	Regulator Type	Input terminal (+3.3V) current Consumption	Output noise / ripple	Transient response
CPU PVPLL	Switching	0.134A	70mV	slower
SAS Controller	Switching	0.167A	69mV	slower
This design on the server motherboard				
Power Source	Regulator Type	Input terminal (+3.3V) current Consumption	Output noise / ripple	Transient response
CPU PVPLL	Hybrid	0.095A	3mV	faster
SAS Controller	Hybrid	0.155A	3mV	faster

IV. CONCLUSION

Server systems complete long time computing operations which vary in time according to different applications. The controllers on the server motherboard still have a control between light loads and heavy loads which thus influences the input terminal power consumption of regulators. In this paper, we design a hybrid LDO regulator and a switching regulator circuit. When the controller is operating in a light load the LDO regulator supplies a current with stable voltage. When the controller is operating a heavy load, this design will automatically swap to the switching regulator in order to supply a stable voltage with current. According to the server motherboard experiment, the input terminal power consumption of this design in comparison with the original design is reduced by 16.94% and the controller continues to operate normally during the swapping. Besides the input terminal power consumption reduction, when the controller operates in a light load, both the output ripple, noise and transient response are all better than in the original design. This design is able to provide better light load efficiency and achieves the purpose of improved power consumption during the operation of the server motherboard.

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